A DECT RF TRANSMITTER WITH INTEGRATED VCO‘s SUITABLE FOR OPEN LOOP GFSK MODULATION

Oliver Kromat[1], Stefan Heinen[1], Udo Matter[1], Giuseppe Li Puma[1], Markus Zannoth[1]

[1]Siemens AG,
EZ D HF, Wacholderstr. 7
40489 Duesseldorf, Germany

Index Terms: GFSK Modulation, Integrated VCO, DECT Transmitter

Abstract-- Since the monolithic integration of VCO‘s complying with the DECT standard seems to be possible the interaction between circuit parts as PLL and Biasing with a fully integrated VCO needs to be studied. This is necessary with the focus on spurious in the output spectrum and the effect on the open loop modulation of the VCO for the generation of a DECT GFSK modulated signal.

I. Introduction

The need to increase the integration density of solid state circuits is growing day by day. This is especially true for the RF part of personal hand held phones. The main goal is not only to reduce the size of the circuit, but also to reduce the test and assembling costs of the whole communication system. The main target is to reduce the equalizing costs of the RF part of the system to zero. One mayor step toward this final would be the fully integration of the VCO. In the past large efforts were undertaken to fulfill wireless standards with integrated VCO‘s [1-3]. All these publications describe stand-alone VCO‘s which are most of the time tunable from the outside and are not subject to other noise sources (except there own) as for example the digital noise from a PLL or a bandgap circuit.

In this paper we will describe the integration of a VCO (including inductors and varactors) with biasing, PLL, output driver and charge pump on a single IC. The influence of the additional circuit parts on the VCO is analyzed. Special focus lies on the open loop modulation of the VCO to form the GFSK output signal which is needed for transmission of the DECT communication signal. This is very important because the output waveform and frequency in the open loop mode depends on the quality of the elements used in the VCO. There should be no large frequency drift or even frequency jumps, when the VCO is modulated

II. The DECT Transmitter IC

The basic concept and realization of this IC is described in reference [4] and a block diagram of the IC is presented in Fig. 1.

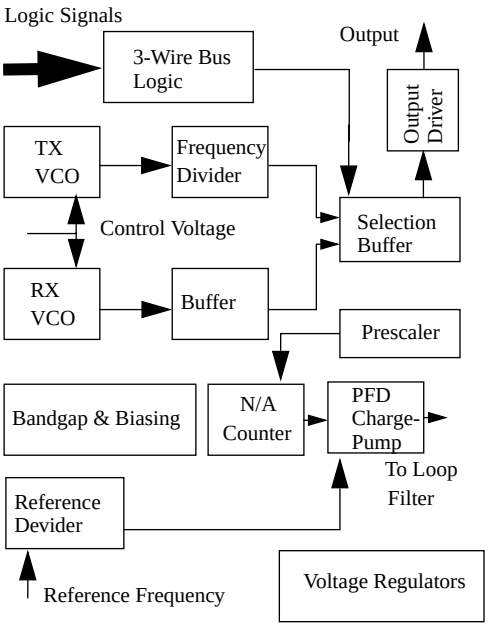

Fig. 1: Block Diagram of the DECT Transmitter

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

The main differences to reference [4] are that the VCO‘s are fully integrated including the varactors and the inductors. There are two VCO‘s implemented. One for transmission and one for receive mode of the IC. The VCO for transmission has a designed center frequency of 1.9 GHz and the one for receive mode of 1.79 GHz. This is another difference to reference [4] where the VCO‘s were running at half the desired output frequency. Though in this design no frequency doublers are used. The output of the VCO‘s are given to a buffer with double input where the selection of transmit and receive VCO signal is implemented, the output of which is connected to the driver output. The driver output power is 0 dBm and it is matched externally to a 50 ohm load.

The output of the selection buffer drives additionally a 32/33 prescaler, the output of which the N and A counter of the PLL counters. The reference frequency is 10.368 MHz, which is divided by 6 to apply a reference frequency of 1.728 MHz (channel spacing in the DECT system) to the phase frequency detector (PFD). The output of the PFD drives the charge pump of the third order PLL. It is possible to set the N counter value between 32 and 35 and the A counter value between 0 and 32.

Also integrated on the IC is the so called 3-wire bus. This bus controls the whole functionality of the RF part of the DECT system. It includes the control signals for the mixers, the LNA, the charge pump and further power control bits of the RX and TX IC‘s.

Furthermore the IC includes two voltage regulators and two bandgap circuits. The regulator circuits contain external bipolar power PNP-transistors to generate the two stabilized power supplies of 3.0 and 2.7 V. The 2.7 V power supply has a PSRR of 60 dB, this is necessary to decouple the VCO from the power supply ripple resulting from the DC/DC converters of the DECT system. Special care was taken to design the second bandgap circuit which is driven from the first regulated power supply; this bandgap references the VCO current, so the generated equivalent output noise voltage needs to be as low as possible.

III. Circuit Descriptions of the VCO‘s

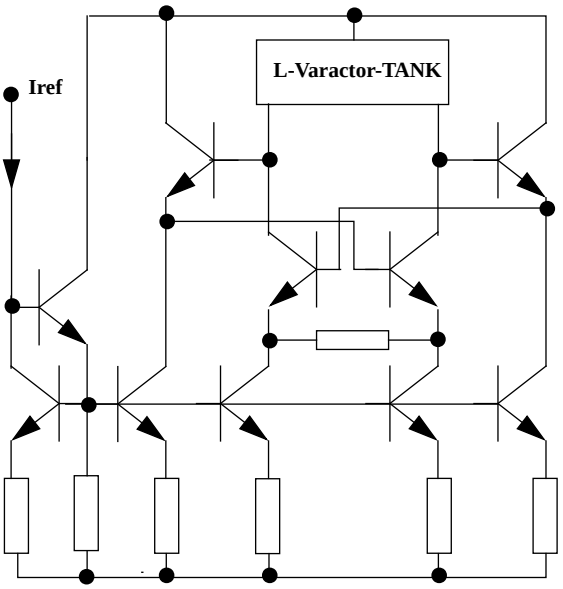

Fig2: Schematic of the VCO

There are two VCO‘s on chip. One for TX the other one for RX mode, because it was not possible to design a wide enough tuning range to only use one VCO for TX and RX. The TX VCO core is running on twice the output frequency, which means 3.7 GHZ. The output of the TX VCO drives a frequency divider, which is implemented as a simple Master Slave D-Flip-Flop, the output of which is given to the RX/TX selection buffer. The RX VCO is running at 1.78 GHz and its output is given to an intermediate buffer before the signal is going also into the RX/TX selection buffer. The reason for designing the VCO‘s on different frequencies, was to find out, if there is an advantage to use a frequency divider. Assuming

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

that both VCO‘s have the same phase noise characteristic at the different operating frequencies, the TX VCO could gain 6 dB in the phase noise characteristic by dividing it‘s output by two.

Both VCO‘s are build from the same concept using a negative impedance converter (NIC) to compensate the losses in the LC tank circuit. The schematic concept of the VCO‘s is displayed in Fig. 2.

The core of the active circuit is a cross coupled pair using emitter followers in the feedback path. The cross coupled pair is degenerated to adjust the excess loop gain of the circuit to the desired value.

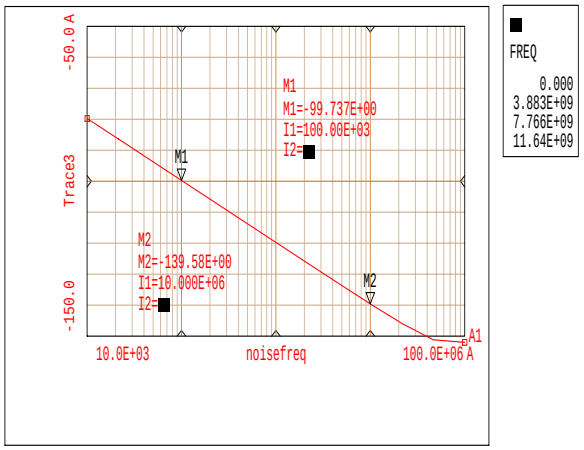

Fig. 3: Phase-Noise Simulation of the TX VCO

The parameters of the active circuit was designed in with use of the MDS software package [5]. Using the extended Leeson formula as a basis [6,7] the designers has several possibilities to influence the phase noise performance of the VCO. The main goals can be summarized as follows:

Increase the Q of the tank; increase the amplitude of oscillation; reduce the noise delivered to the tank (biasing noise and noise of the active circuit), choose the excess loop gain near unity; use fast transistors. Designing for this goals and using MDS the simulated phase noise of the VCO with biasing came out to be -139.5 dBc @ 10 MHz for the TX-VCO (in front of the frequency divider) and 137.3 dBc @ 5 MHz for the RX VCO. Fig. 3 displays one of the simulated results.

IV. Measurements

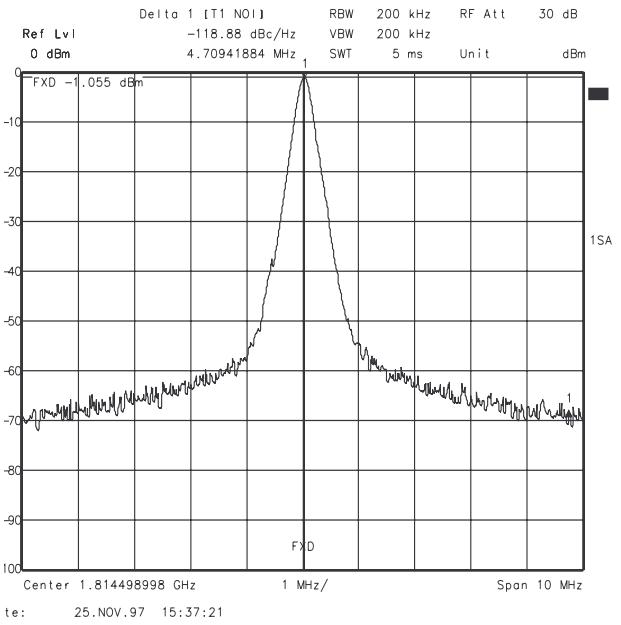

Fig.4: Measurement of VCO Phase-Noise

After the IC, packaged in a TSSOP28 plastic package, was assembled on a test board the following measurements could be performed. The main on-board components are a balun for the differential output driver, the loop filter, the power pnp transistors and decoupling capacitors for the different supply lines. First, the VCO’s were measured in the open-loop mode and the phase noise came out to be 119 dBc/Hz @ 4.7 MHz for both VCO’s respectively (Fig. 4).

This is a mayor offset from the simulation results, that we could not explain with a wrong modeling of device parameters. After this measurement the VCO was brought into the closed loop mode. In the output spectrum the reference side bands (1.728 MHz) appear at 65 dBc. No further spurs except at 10.368 MHz (also 65 dBc) could be observed from the PLL, so that we can conclude, that the implemented realization of the PLL in ECL-technique is not influencing the VCO‘s in any way. After this satisfactory measurement the VCO was analyzed within a DECT burst. That means that the VCO is switched between open- and closed-loop mode on a single DECT channel. The result is displayed in Fig.5.

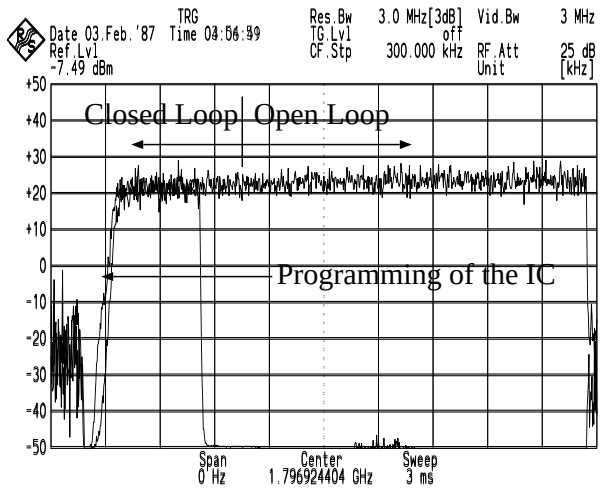

Fig 5: Open Loop Frequency Behavior

No frequency offset or mayor frequency drift was observed in the output frequency in the open loop mode compared to the closed loop mode. Even the influence of the 3-wire bus programming which could be observed in [4], is strongly degraded with the integration of all VCO elements.

V. Summary

A fully integrated VCO working in a DECT transmitter environment has been presented. The measurement of the fully integrated VCO, including inductor, varactor, biasing and active circuit, showed no major influence by other circuit parts like the PLL. Even the interference caused by on-board components, which could be observed in a previous design [4], could be reduced. These interferences were mainly due to the off-chip resonator tank of the VCO. Nevertheless, it will be a long way to go to meet the DECT system requirements for the VCO in an integrated environment, especially when there is no correlation between simulated and measured parameters.

VI. References

[1] B. Jansen, Don Lee, Kevin Negus: "Silicon bipolar VCO family for 1.1 to 2.2 GHz with fully-integrated tank and tuning circuit", ISSCC 97, Digest of Technical Papers, pp. 392-393, San Francisco 1997.

[2] L. Dauphinee, M. Copeland, P. Schvan: "A balanced 1.5 GHz voltage controled oscillator with integraed LC resonator", ISSCC 97, Digest of Technical Papers, pp. 390-391, San Francisco 1997.

[3] J. Craninckx, M. Steyaert: "A CMOS 1.8 GHZ low phase noise voltage controlled oscillator", ISSCC 95, Digest of Technical Papers, pp. 266-267, San Francisco 1995.

[4] S. Heinen et al: "An Integrated Bipolar Transmitter for DECT", RFIC Symposium, Digest of Technical Papers, pp. 127-130, San Francisco 1997.

[5] HP EEsof; Microwave Design System (MDS) Version 7.0

[6] C. A. M. Boon: "Design of high-preformance negative feedback oscillators", PhD. Thesis, Delft University, The Netherlands, 1989.

[7] D. B. Leeson: "A simple model of feedback oscillators noise spectrum", Proc. IEEE, Vol. 52, No. 2, 1966.